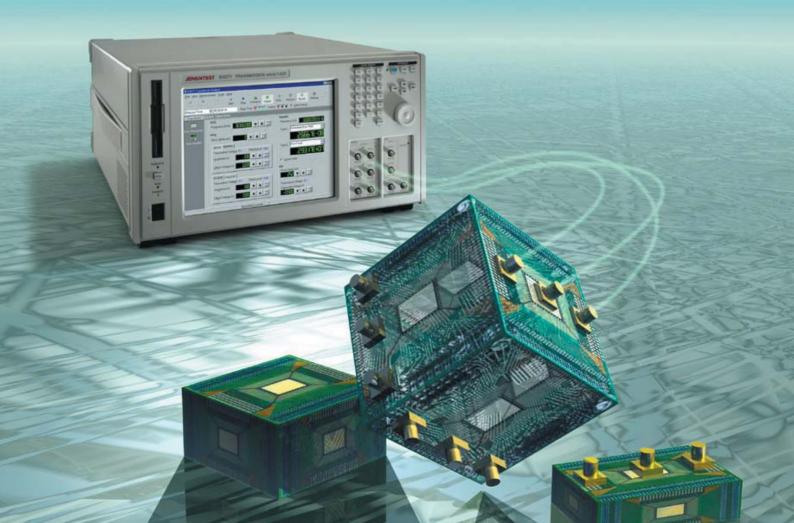


D3371 3.6 GHz Transmission Analyzer

Compact Integration of a Pulse Pattern Generator and Bit Error Detector.

Wide Variety of Measurement Options for Gigabit Ethernet and SONET/SDH.





The volume of communications data on the Internet has been growing very quickly. This has caused a continuing rapid expansion of capacity in backbone networks and computer networks.

The D3371 Transmission Analyzer has a variable data rate capability from 10 MHz to 3.6 GHz which encompasses all data rates necessary for SONET/SDH, Fiber Channel, and Gigabit Ethernet devices required for the IP network markets. It can also generate various types of PRBS and user programmable test patterns for simulating actual line traffic, enabling flexible accommodation of a wide range of needs from development to production and ongoing maintenance.

- Excellent output waveform quality
- 3 Vp-p maximum, wide range of output amplitudes from lowamplitude devices to direct Laser Diode modulation and Electro Absorption modulators
- Capability to generate diverse test patterns for Gigabit Ethernet and SONET/SDH
 - Pseudo random (PRBS) pattern
 - Programmable pattern
 - Zero substitution pattern
 - STM (SONET/SDH) frame pattern
 - Flexible pattern

• Significantly enhanced bit error measurement functions

- Error rate measurement
- Error count measurement
- Error interval measurement
- Error-free interval measurement
- Frequency measurement
- Error performance measurement
- Burst pattern signal generation capability
- High-precision 10 MHz to 3.6 GHz internal synthesized clock generator
- Auto search function
- GPIB Remote control function
- 10Base-T Ethernet interface
- Interactive GUI with large color LCD, touch panel

Windows® application software

Free, non-warranted software provides these capabilities.

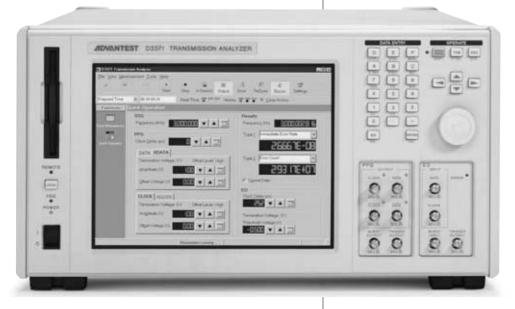
- 8B/10B code editor software for Gigabit Ethernet pattern creation
- Pattern editor/converter software enabling easy data creation
- Q-FACTOR measurement, Eye margin measurement, and BER (Bit Error Rate) diagrams measurement software

Module options

- OPTION 10: Pulse Pattern Generator (2 Vp-p output) module
- OPTION 11: Pulse Pattern Generator (3 Vp-p output) module
- OPTION 12: Error Detector module
- OPTION 13: 3.6 GHz synthesizer module

Measurement function options

- OPTION 70: Jitter Tolerance option
- OPTION 71: Pattern option
- OPTION 72: Error phase analysis option



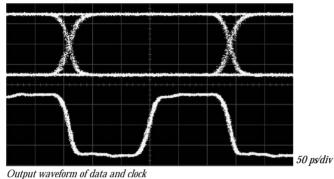
Pulse Pattern Generation Module (OPTION 10: 2 Vp-p output) (OPTION 11: 3 Vp-p output)

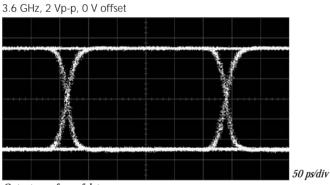
Pulse Pattern Generation Function

Optimum for evaluating devices and module characteristics

High-quality data patterns can be generated for evaluating the characteristics of optical devices (requires user supplied E/O and O/E optical interfaces) and sub-systems for data communications. It is possible to generate a maximum of 8 M-bits of user programmable patterns, PRBS patterns (2⁷-1 to 2³¹-1, with adjustable Mark/Space ratio), and user settable zero substitution patterns. It is also easy to vary the amplitude, offset and cross point for the output data and clock waveform.

3.6 GHz, 1 Vp-p, 0 V offset

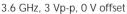


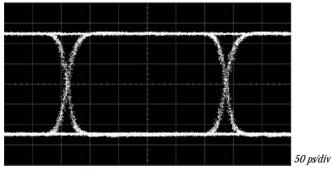


Output waveform of data

The Pulse Pattern Generator has a wide output range suitable for evaluation of Electro Absorption modulators and Laser Diodes

It is easy to output patterns to suite various types of devices from low-amplitude devices to high-level input EA modulators. (max. 3 Vp-p output: OPTION 11)





Output waveform of data

Easy Set Up for Pulse Pattern Generator

The pattern generator section settings can be changed or verified with ease using the common MS Windows and touch screen interface. Burst data can also be easily output. The interface is also applicable to ECL/LVPECL/CML and GND termination.

Settings	X
Module :	PPG
10 A A A A A A A A A A A A A A A A A A A	Data Clock Pattern Burst Error Addition Trigger/Aux
SSG	Track Data
PPG	DATA XDATA
ED ED	Enable DATA Quiput Cross Point 50 %
System	Iermination Amplitude 0.80 V
	to GND (0V) Offset € High 0.00 V
	ECL(-2V) C Middle 0.40 V
	LVPECL (+1.3V)
	CML Termination ⊻oltage
	0 V
	OK Cancel Apply

Example setting of Pulse Pattern Generator

Easy Creation of Programmable Patterns

Using the internal pattern editor enables to easily construct, store and recall data patterns up to approximately 8 M-bits in length. It is also possible to store and recall a pattern created on an external personal computer via GPIB or floppy disk.



Example display of Programmable Pattern editor



Pulse Pattern output connector

Error Detector Module (OPTION 12)

Bit Error Measurement Function

Automatic Setting of Optimum Measurement Values using the Auto Search Function

The Auto Search Function allows for automatically setting the PRBS pattern, input data threshold voltage and input clock phase to values optimum for measurement. It is also possible to conduct measurements on a test system with a large error rate (about 10^{-2}) by optionally setting the synchronization determination threshold value. In addition, combining the Error Detector module with the Pulse Pattern Generator module enables bit error measurement using burst data, allowing easy execution of a loop-back test with optical fiber cable. It is also possible to save the measurement result logs in text file form.

😂 日 Open Save A	s Print Start	Stop A-Searc		成 的 Error ReSync	- ⊈: Buzzer Setti	
Elapsed Time	▼ 00 00:00:19	Real Time: ERR S	YN CLK History:	eer syn cyk 🗙 🖂	ear History 👫 🖁	l.
Functions	asic Measurement					
sic Measurement	Frequency 2,500	1,000,384 Hz				
	Results	Omitting	Inserting	Total	B1	Total
1000	Bit Count	2.3751E+10	2.3749E+10	4.7500E+10	Bit Count	****
₩ 0	Error Rate	6.3156E-10	6.3160E-10	6.3158E-10	Error Rate	****
Quick Operation	Error Count	1.5000E+01	1.5000E+01	3.0000E+01	Error Count	****
	Immediate Error Rate	0.0000E-08	0.0000E-08	0.0000E-08		
	Immediate Error Count	0.0000E+00	0.0000E+00	0.0000E+00		
or Phase Analysis	Error Intervals	7.8947%	7.8947%	15.2632%		
	Error Free Intervals	92.1053%	92.1053%	84.7368%		
	Performance	Total	Threshold	Threshold El	Threshold EFI	
Jitter Tolerance	Error Seconds	36,84213	> 1E - 3	0.0000%	100.0000	
	Error Free Seconds	63,1579%	> 1E - 4	0.0000%	100.0000	
	Severely Errored Seconds	0.0000%	> 1E - 5	0.0000%	100.0000	
	Unavailable Seconds	0.0000%	> 1E - 6	0.0000%	100.0000	
	Degraded Minutes		> 1E - 7	0.0000%	100.0000	
			> 1E - 8	0.0000%	100.0000	
	Results	Total	<= 1E - 8	15.2632%	84,7368	
	Clock Loss Intervals	0				
	Sync Loss Intervals	0				

Example display of Basic Measurement result

State .	Jitter Tolerance		Specific Field	
SSG	Trigger / Aux Log	Condition	Display Format	Buzzer
1	Data Clock	Pattern Syn	C Auto Search	Mask
PPG	Auto Sync			
Tim ED	Sync Pattern Length	2 💌 bit		
	Sync PR <u>O</u> G Address	bit		
	Sync FLEX Index			
	Sync FLEX Address	bit		
	Auto Threshold			
	Sync Gain Threshold	Sy	nc Loss Threshold	
	PRBS 1E-2	▼ P <u>F</u>	BS 1E-2	-
	Mgmory 1E-4	▼ Me	mory 1E-4	Ψ.

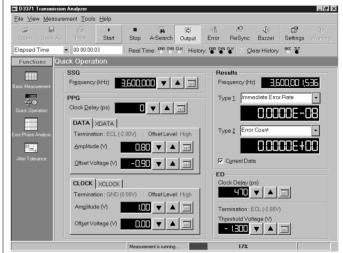
Setting display of synchronization threshold

Masked Data Measurement

By specifying the measurement start bit and measurement stop bit, it is possible to measure the bit error rate of only specific bits of the data received by the error detector. In addition, with the pattern option (OPTION 71), it is also possible to measure the bit error rate of specific bits of the STM (SONET/SDH) frame or flexible patterns.

Easy Setting of Basic Measurement Conditions in the Quick Operation Window

The Quick Operation window is provided so that the user can easily set up and execute the basic measurement conditions. The frequently varied measurement condition settings and the measurement results can be visually confirmed enabling easy operation.



Example display of Quick Operation

3.6 GHz Synthesizer Module (OPTION 13)

The synthesizer module (10 MHz to 3.6 GHz) can be installed to provide an internal high-frequency resolution, high accuracy, and reduced SSB phase noise clock source.

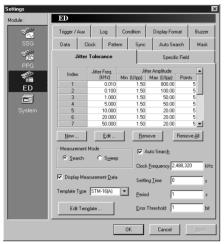
lule :	SSG
1	Frequency
SSG	Clock
	🔽 Qutput
	Erequency 2.500,000 kHz
	Reference: Internal C External
ED	Litter Modulation
System	Frequency 10 Hz
	Amplitude 0.00 Ulpp

Setting display of synthesizer module

Jitter Tolerance Option (OPTION 70)

Jitter Tolerance Measurement Function

By setting the jitter frequency to be added, jitter amplitude value (minimum value and maximum value), and the number of measurement points with respect to the specified clock frequency, jitter tolerance measurements can be performed. However, it is necessary to use the Pulse Pattern Generator module (OPTION 10/11), Error Detector module (OPTION 12), and 3.6 GHz Synthesizer module (OPTION 13).



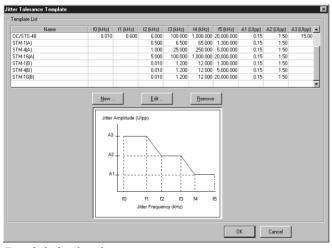
Setting display of jitter tolerance measurement

Measurement Using User-Defined Templates

OC/STS-1, 3, 12, and 48^{*} and STM-1, 4 and 16^{**} can be selected as a default template for jitter tolerance measurement. Measurement using user-defined templates is also possible.

*: Reference standards: Bellcore GR-253-CORE

**: Reference standards: ITU-T G.958



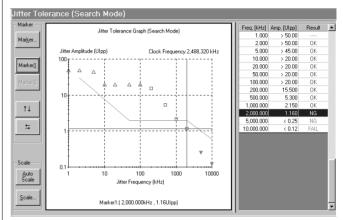
Example display of template

Graphical Display of Automatic Measurement of Jitter Tolerance

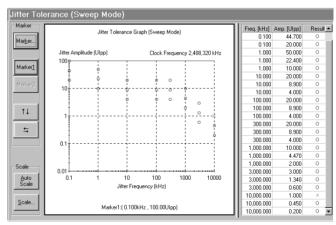
The jitter tolerance is measured automatically by setting the jitter tolerance measurement condition. The result is displayed using a graph and table.

In addition, automatic pass/fail and display is possible by setting the error threshold (bit error value) for pass/fail determination. In the Search mode, the jitter tolerance point is automatically detected from measurement points specified for each jitter frequency and displayed.

In the sweep mode, the software judges whether the value is equal to or smaller than the error threshold (bit error value) or not (pass or fail) at all the specified measurement points.



Example display of Search Mode Measurement



Example display of Sweep Mode Measurement

Pattern Option (OPTION 71)

STM (SONET/SDH), Flexible Pattern Function

There are two different Pattern options: STM (SONET/SDH) pattern and FLEX pattern. Pattern options are used together with the Pulse Pattern Generator module (OPTION 10/11) and Error Detector module (OPTION 12).

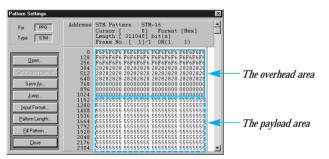
In the STM (SONET/SDH) pattern, it is possible to easily create data with the frame structure conforming to ITU-T G.707 recommended. For the overhead area, any data pattern created by the programmable pattern creation function can be used. For the payload area, a programmable pattern or PRBS pattern can be selected. In addition, it is possible to set B1 insertion and scramble addition conforming to ITU-T G.707 recommended.

Overhead error, payload error, and B1 error measurement can also be performed.

Settings	X
Module :	PPG
100 A	Data Clock Pattern Burst Error Addition Trigger/Aux
SSG	Pattern Polarity
1	Normal O Inverted
PPG	
	Pattern Type STM
ED	i dicenti The
	STM
System	Insert PRBS into Payload
	Pattern Length 2^31 - 1 bit
	Mark Ratio 1/2
	□ Scramble
	☐ Insert <u>B</u> 1
	Pattern Settings
,	
	OK Cancel Apply

Example display of STM (SONET/SDH) pattern setting

The STM (SONET/SDH) pattern creation screen allows creation of the overhead area and payload area.



Example display of STM (SONET/SDH) pattern creating

It is possible to create a FLEX pattern through the combination of the Programmable pattern and PRBS pattern. The combination, generation order, and generation bit length can be defined in the pattern sequence table.

This function makes it possible to easily create an IP header and IP data with the PRBS pattern used in the data section. By using the error phase analysis function (OPTION 72), it is possible to locate the errored bit position of the IP data.

Module :	PPG
ssg	Data Clock Pattern Burst Error Addition Trigger/Aux
*	Pattern Polarity © Normal © Inverted
PPG	Pattern Type FLEX
System	FLEX-
	PROG Patern No. 1
	Pattern <u>S</u> ettings
	PBBS Pattern Length 2^7 - 1 tot
	Mark Ratio
	OK Cancel Apply

Example display of FLEX pattern setting

Pattern Sequence Table	;			×
For PPG	Index	Pattern	Length (bit)	FLEX Trigger
FOI THO	1	PROG002	320	Low.
Type FLEX	2	PROG001	128	High
	3	PRBS	256	Low
	4	PR0G003	192	Low
Open	5	PROG001	128	Low
	6	PRBS	512	Low
Set Seq. Memory	×			
Save <u>A</u> s				
New				
Edit				
<u>R</u> emove				
Default				
Close				

Example display of FLEX pattern creating

Error Phase Analysis Option (OPTION 72)

Error Phase Analysis Function

Error phase analysis is used together with the Error Detector module (OPTION 12). It is performed at the same time as the bit error measurement to continuously record bit error positions. By analyzing the errored bit position information after completion of a bit error measurement, the causes of the bit error(s) may be more easily determined.

In addition, errored bits in a specific area can also be recorded. The result of an error phase analysis can be displayed in time sequence or statistical form.

Displaying Result in Time Sequence

The pattern information and error bit position are displayed in time sequence. The PRBS pattern contained in the STM (SONET/SDH) pattern or FLEX pattern can also be displayed. Usable patterns include the programmable pattern, Zero Substitution pattern, STM (SONET/SDH) pattern and FLEX pattern. The PRBS pattern cannot be used separately.

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Cycle No	Address											B	at	te	-2-3	1	(B:	in	ar:	y)								ē		÷	
0000002	0000000	1	1	1	1	1	1	1	0	0	0 0	0	0	1	0	0	0	0	1	1	0	0	0	0	1	0	1	0	0	0	i 💻
0000002	0000032	1	1	1	0	0	1	0	0	0	1 0	1	1	0	0	1	1	1	1	0	1	0	0	1	1	1	1	1	0	1	o 🛧
0000002	0000064	0	0	0	1	1	1	0	0	0	1 0	0	1	0	0	1	1	ο.	1	. 0	1	0	1	1	0	1	1	1	1	0	1
0000002	0000096	1	0	0	0	1	1	0	1	0	0 1	. 0	1	1	1	0	1	1.	L	0	1	1	0	0	1	0	1	0	1	0	o 🐳
0000002	0000128	0	0	0	1	0	0	0	1	0	0 0	1	0	0	0	1	0	0		0	0	1	0	0	0	1	1	0	0	1	1
0000002	0000160	0	0	1	1	0	0	0	0	0	10	1	0	0	1	0	0	1	0	0	1	0	1	1	0	0	0	0	1	0	1
0000002	0000192	1	0	0	1	0	0	1	0	0	0 0	1	0	0	1	1	0	ο.	LC	0	1	1	0	0	0	1	1	0	0	1	1 .
0000002	0000224	0	0	0	0	0	0	0	0	0	0 1	. 1	0	1	1	0	0	0	1	L O	0	0	1	0	0	1	1	0	0	1	1 Jun
0000002	0000256	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	1	0	0
0000002	0000288	0	1	0	1	0	1	0	0	0	1]	. a	0	0	1	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0
0000002	0000320	0	0	0	1	0	0	1	0	0	1 0	1	0	0	1	0	0	1	1	1 0	0	0	1	0	0	0	1	0	0	1	o 🖵
0000002	0000352	1	1	1	1	1	1	1	1	1	1]	. 1	1	1	1	1	1	ο.	ιc	1	0	1	0	1	0	1	0	1	0	1	0 ERF
0000002	0000384	1	0	1	0	0	0	0	0	0	1 0	1	0	1	0	0	0	1	1	1 0	0	0	1	1	1	1	1	0	0	0	0
0000002	0000416	0	0	1	0	0	1	0	1	0	0 0	0	1	0	1	0	0	ο.	L	0	0	0	0	1	0	1	0	0	1	0	1
0000002	0000448	0	0	1	0	0	1	0	1	0	0]	. 0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	0
0000002	0000480	0	1	0	1	0	1	0	1	0	0 0	0	1	1	0	0	0	ο.	L	0	1	0	1	0	0	1	0	0	0	4	0
0000003	0000000	1	1	1	1	1	1	1	0	0	0 0	0 0	0	1	0	0	0	0	1	1	0	0	0	0	1	0	1	0	0	0	1
0000003	0000032	1	1	1	0	0	1	0	0	0	1 0	1	1	0	0	1	1	1	1	. 0	1	0	0	1	1	1	1	1	0	1	0
0000003	0000064	0	0	0	1	1	1	0	0	0	10	0	1	0	0	1	1	ο.	1	0	1	0	1	1	0	1	1	1	1	0	1
0000003	0000096	1	n	n	n	1	1	0	1	n	0.1	lo	1	'n	1	n	1	1	i i	0	1	1	n	0	1	0	1	0	1	0	0

Example display of Error phase analysis (Time Sequence display)

Displaying the Result in Statistical Form

The statistics data display includes the number of bit errors and bit rate for each bit of the pattern. Error bits are displayed in different colors for each bit error rate.

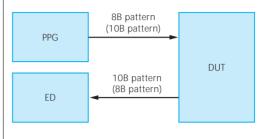
			-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-			-	-	-	-	=	7			
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rame No	Row	Column											E	?a1	EE	•x	n	()	51	a	Y	2								i	æ	æ		
001	1	0101	0	0	0	1	1	1	0	1	1	1]	L C	0	1	0	1	1	0	0	0	1	1	ι.	1	1	1	1	0	0	0	0	1	
001	1	0105	1	1	1	0	0	1	0	1	1	0 0	1	0	0	1	1	1	1	1	0	0	0	О.	1	1	1	0	1	1	1	0	1	1
001	1	0109	1	0	0	1	0	0	1	0	0	0 0	1	. 1	0	0	1	1	1	0	1	1	1	L	0	0	1	1	0	0	0		0	T
001	1	0113	0	0	0	0	0	1	0	1	1	0	c	1	1	1	0	0	1	0	1	1 1) :	L I	0	1	1	1	0	0	1	0	0	Ť
001	1	0117	0	1	0	1	0	0	0	1	1	0 1	1	. 1	0	0	1	0	0	0	1	1 1) :	ι.	1	1	0	0	0	1	1	0	1	V
001	1	0121	1	0	1	1	1	0	0	0	1	1 1	. 0	0	0	1	1	1	0	0	0	1	1	L.	1	1	1	0	0	0	0	0	0	<u> </u>
001	1	0125	1	1	1	1	1	1	1	1	1	1 1	. 1	. 1	1	1	1	1	1	1	0	0) :	ι.	1	1	0	0	0	1	1	1	0	
001	1	0129	0	0	0	0	0	0	0	0	0	0 0	0	0	0	0	1	1	1	1	1	1	1	ι.	1	1	1	1	1	1	1	0	0	Jump
001	1	0133	0	0	0	0	0	0	0	0	0	0 0	1	. 1	. 1	0	0	0	0	0	0	9	0	0	0	0	0	1	1	1	0	0	0	
001	1	0137	0	0	0	0	0	0	0	1	1	1 1	. 1	. 1	0	0	0	0	0	0	0	9) :	ι.	1	1	1	1	1	0	0	0	0	EBB
001	1	0141	0	0	0	1	1	1	0	0	0	1 1	1	. 0	0	0	0	0	0	1	1	1	0	0	0	1	1	1	0	0	0	0	1	Ī
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001	1	0149	٠	٠	٠	٠	٠	٠	٠	•	٠	• •	• •		•	٠	٠	٠	٠	٠	٠	•	•	٠	٠	٠	٠	٠	٠	٠	٠	٠	٠	I I I I I
001	1	0153	٠	*	٠	٠	٠	٠	٠	٠	٠	•	• •			٠	٠	٠	٠	٠	٠	•	•	٠	٠	*	٠	٠	٠	٠	٠	٠	٠	 16
001	1	0157	*	*	٠	•	•	*	*	2	٠	• 6		2										×	4							٠		
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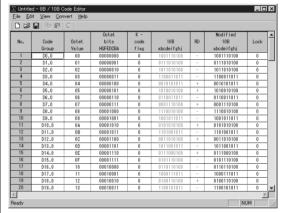
Example display of Error phase analysis (Statistics Display)

Wide Variety of Windows Application Software

8B/10B code Editing Function for Gigabit Ethernet

By using the 8B/10B code editor function, user-defined 8 bit patterns can be converted to 10 bit patterns automatically. Since the created 8 bit pattern and 10 bit pattern can be used with the pulse pattern generation function, the 10 bit pattern can easily be transferred to devices, modules, and communication equipment for Gigabit Ethernet. In addition, the 8 bit pattern and 10 bit pattern can also be used with the error detector function.





Example display of 8B/10B code editor function

Pattern Editor Function

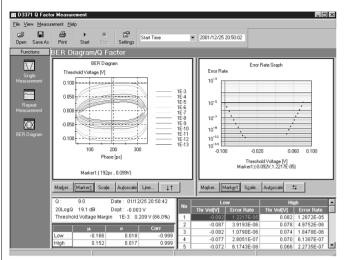
Although any patterns can be created and edited directly on the D3371, the use of the external pattern editor software makes it easier to create and edit patterns on a PC.

_	Pat	_	b 6	_	(-16	_	<u>.</u>	01	0.1	1	_	_	_	_	_	_	_	_	_	_	_	-
0 +0	+1	+2	n +3	+4		ری +6	+7	не м +8	0.1. +9	10 +0	+1	+2	+3	+4	+5	+6	+7	+8	+9	20 +0	+1	+2
Å1	À1	λ1	Å1	Å1	λ1	Å1	Α1	λ1	Δ1	∆1	À1	Å1	41	À1	À1	∆1	Α1	À1	Δ1	Δ1	λ1	Δ1
F6 B1	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6	F6
00 D1	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00 H1	00 H1	00 H1	00 H1	00 H1	00 H1	00 H1	00 H1	00 H1	00 H1	00 H1	00 H1	00 H1	00 H1	00 H1	00 H1	00 H1	00 H1	00 H1	00 H1	00 H1	00 H1	00 H1
00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2
00 D4	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00 D7	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00 D10	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00 51	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	0.0

Example display of pattern editor function

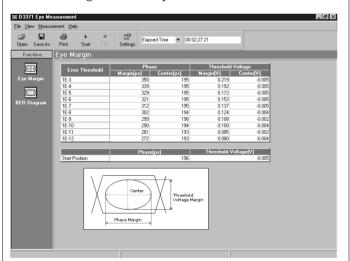
Q-FACTOR Measurement, Eye Margin Measurement, and BER Diagrams Measurement Functions

Using a GPIB connection to a Windows-based PC to control the D3371, Q-FACTOR measurement, Eye margin measurement, and BER diagrams measurement can be performed. In a Q-FACTOR measurement, the "threshold voltage vs. bit error rate" can be displayed.



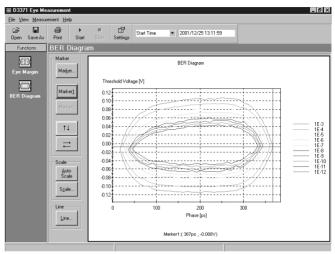
Example display of Q-FACTOR measurement result

In the Eye margin measurement, the phase margin and threshold voltage margin are measured while varying the phase and threshold voltage so that the specified error rate is not exceeded.



Example display of Eye margin measurement result

In a BER diagram measurement, points of the specified error rate are connected and displayed while varying the threshold voltage and phase. As an application of Q-FACTOR measurement, it is also possible to perform BER diagrams measurement by measuring the error rate for a short time.



Example display of BER diagrams measurement result



Specifications

D3371 Main Unit System Function

Sy	st	er	n	F	u	nc	τι	0	
	_	_	_	_	_	_	_	_	7

OS:	Microsoft [®] Windows 98 Second Edition
Main memory:	128 MB
Display unit:	10.4 inch TFT LCD color display with the touch
	panel functions 800 x 600 pixels, with a back-light
Floppy disk drive:	3.5 inches in two modes (720 KB/1.44 MB)
Hard disk:	3.5 inches (6 GB or more)
Operating part:	Panel keys and the touch panel
Remote control:	GPIB compliant with IEEE 488.2
Measurement time	
base accuracy:	±10 ppm

Input/Output

Parallel connector:	D-sub25 pins
USB connector:	Type A connector,
	2 channels installed for the keyboard and mouse
Ethernet connector:	10 Base-T
GPIB Connector:	IEEE 488.2 bus connector

General Descriptions

Operating	
environment range:	+5 to +40°C
-	Relative humidity;
	40 to 85% (without condensation)
Storage	
environment range:	-20 to +70°C
-	Relative humidity;
	30 to 85% (without condensation)
AC input power source:	100 VAC and 200 VAC systems are switched automatically
	100 VAC system operation; 100 to 120 V, 50/60 Hz
	200 VAC system operation; 220 to 240 V, 50/60 Hz
Power consumption:	160 VA or below
Mass:	21 kg (46.3 lbs.) or less
	(module, accessories, and so on are not included)
Dimension:	Approximately 424 (W) x 221 (H) x 500 (D) mm
	(approximately 16.7 (W) x 8.7 (H) x 19.7 (D) in.)
	(the protrusions of the rear feet, connectors,
	and so on are not included)



2 Vp-p or 3 Vp-p Output Module of the Pulse Pattern Generator (PPG Module)

(2 Vp-p Output: OPTION 10, 3 Vp-p Output: OPTION 11, Pattern: OPTION 71)

Generated Pattern

Generated Pattern					
Pseudo random (PRBS) p Pattern length: Number of stages and		7, 9, 1	0, 11,	15, 23, 31)	
generating function:	Number of stages			St	andard
	7	X ⁷ + X			mended V. 29
	9	X ⁹ + X X ¹⁰ + X		ITU-T recom	mended V. 52
	10 11			ITU-T recom	mended O. 152
	15	X ¹⁵ + X	X ¹⁴ + 1	ITU-T recom	mended O. 151 (1/2)
	23			ITU-T recom	mended O. 151 (1/2)
	31	X ³¹ + X			
Mark ratio (variable): Mark ratio and number of bit shift:	1/2, 1/4, 1 bit	1/8, 0)/8, 1/	2, 3/4, 7/8,	8/8
Programmable (PROG) p. Pattern length: Pattern length and variable setting	1 to 8,38	38,608	(2 ²³) I	bit	
resolution [bit]:	Patt	ern le	ngth	range	Setting resolution
		262,1 146 to		200	1
		292 to			4
				97,152	8
				94,304 88,608	16 32
Zero substitution (ZSUB) Pattern length: Continuous zero bit length and setting			-	-	
resolution [bit]:	length			nuous zero ngth range	Setting resolution
	2' 2'			to 127	1
	2 2 ¹⁰			to 511) to 1023	1
	2 ¹¹			1 to 2047	1
	2 ¹⁵		1!	5 to 32767	1
STM (SONET/SDH) patter					
Frame structure: Number of frames:	STM-4, S STM-4; 1			nes	
Number of frames.	STM-16;				
Payload types:	Can be selected from PROG pattern and PRBS				
Scrambling:	pattern Can be p	novid	ed		
B1 byte:	Can be p				
Flexible (FLEX) pattern (OPTION 7	1)			
Number of patterns:	PROG pa	attern			
Pattern length:	PRBS pa			e to 65,536 bi	ts
r attern tengtn.	(setting	resolu	ition:		
	(setting				
Number of combined patterns:	1 to 102	4 patt	ern(s)		
Pattern logic:	Can be l	ogical	ly inv	erted	
Error Addition					
Mode: Error addition route:	Repeat, Route; 1			External	
Burst					
Mode:	Internal	gener	ation	burst, Exte	rnal burst

Trigger	
Mode:	Can be selected from the 1/8 clock, 1/32 clock, pattern phase, Frames (OPTION 71)
Pattern phase:	and Flexible (OPTION 71) PRBS Pattern; output position can be varied in increment of 1 bit PROG Pattern; output position can be varied in
	increment of 16 bit ZSUB Pattern; output position can be varied in
Frames (OPTION 71):	increment of 16 bit Output position can be set for each frame
Flexible (OPTION 71):	separately on a 16 bit basis The Low level or High level can be set for each pattern
AUX	
Data types:	The Low level is output for PROG pattern The High level is output for PRBS pattern
Clock Input	
Input amplitude: Input waveform:	0.5 to 2 Vp-p Rectangular wave or Sine wave (175 MHz to 3.6 GHz) Rectangular wave (10 to 175 MHz)
Duty ratio: Input impedance: Connector:	$50 \pm 5\%$ 50Ω (nominal) to 0 V SMA female
Data Output	
Frequency:	10 MHz to 3.6 GHz 2 paths (each of DATA and DATA) NRZ DC
Amplitude range 2 Vp-p output module (OPTION 10)	
3 Vp-p output module	To CND.
(OPTION 11): Offset range:	To GND; 0.3 to 2 Vp-p setting resolution: 10 mV (OPTION 10) 0.3 to 3 Vp-p setting resolution: 10 mV (OPTION 11) ECL (to -2V); 0.6 to 1 Vp-p setting resolution: 10 mV LVPECL (to +1.3 V); 0.6 to 1 Vp-p setting resolution: 10 mV CML (to Vcc); 0.3 to 1 Vp-p setting resolution: 10 mV Exception; Vcc (termination voltage) is set between 0 and 3.5 V in 50 mV setting resolution To GND; -2.0 to +2.0 V (High) setting resolution: 10 mV ECL (to -2.0 V; -1.0 to -0.6 V (High) setting resolution: 10 mV LVPECL (to +1.3 V); +2.3 to +2.7 V (High) setting resolution: 10 mV CML (to Vcc); Vcc -0.2 V to Vcc +0.2 V (High) setting resolution: 10 mV Exception; Vcc (termination voltage) is set
Display: Rise and fall times: DATA/DATA tracking function: Variable cross-point: Load impedance: Connector:	between 0 V and 3.5 V in 50 mV setting resolution When the amplitude setting exceeds 2 Vp-p; -1.0 to +1.0 V (High) setting resolution: 10 mV (to 0 V) Can be switched to High, Middle, Low 60 ps (10 to 90%) or less (output amplitude \geq 0.5 Vp-p) 80 ps (10 to 90%) or less (output amplitude <0.5 Vp-p) Yes. User selectable Yes. User selectable 50 Ω SMA female

Number of	
output paths:	2 paths (each of CLOCK and CLOCK)
Coupling:	DC
Amplitude range:	To GND; 0.3 to 2 Vp-p setting resolution: 10 mV
	ECL (to -2 V); 0.6 to 1 Vp-p setting resolution: 10m
	LVPECL (to +1.3 V);
	0.6 to 1 Vp-p setting resolution: 10mV CML (to Vcc);
	0.3 to 1 Vp-p setting resolution: 10mV
	Exception; Vcc (termination voltage) is set betwee
	0 V and 3.5 V in 50 mV setting resolution
Offset range:	To GND;
	-2.0 to +2.0 V (High) setting resolution: 10mV
	ECL (to -2 V);
	-1.0 to -0.6 V (High) setting resolution: 10mV
	LVPECL (to +1.3 V); +2.3 to +2.7 V (High) setting resolution: 10mV
	CML (to Vcc); Vcc -0.2 V to Vcc +0.2 V (High) setting
	resolution: 10 mV
	Exception; Vcc (termination voltage) is set betwee
	0 V and 3.5 V in 50 mV setting resolution
Display:	Can be switched to High, Middle, Low
Rise and fall times:	60 ps (10 to 90%) or less
	(output amplitude ≥0.5 Vp-p)
	80 ps (10 to 90%) or less (output amplitude <0.5 Vp-p)
Clock delay:	±1 ns (setting resolution: 1 ps)
Load impedance:	50Ω
Connector:	SMA female
Burst Input	
Input level:	0/-1 V
Input impedance:	50 Ω (nominal) to 0 V
Connector:	SMA female
Burst Output	
Output level:	0/-1 V
Load impedance:	50Ω to 0 V
Connector:	SMA female
Error Input	
Input level: Input impedance:	0/-1 V 50Ω (nominal) to 0 V
Connector:	SMA female
Trigger Output	0/11/
Output level: Load impedance:	0/-1 V 50Ω to 0 V
Connector:	SMA female
General Description Operating	13
environment range:	+5 to +40°C
	Relative humidity;
	40 to 85% (without condensation)
Storage	•
environment range:	-20 to +70°C
	Relative humidity;
Doutor con-	30 to 85% (without condensation)
Power consumption: Mass:	120 VA or below 6.0 kg (13.2 lbs.) or less

Frror Detector Module	(ED Module: OPTION 12,	Received Pattern					
	or Analysis: OPTION 72)	Frequency:	10 MHz to	3.6 GF	Ηz		
Measurement		Pseudo random (PRBS) p		0.0 0.			
Error rate:	0.0000 x 10 ⁻¹⁷ to 1.0000 x 10 ⁻⁰	Pattern length: Number of stages and		9, 10,	11, 15, 23, 31)		
Error count: Error interval (EI):	0 to 4294967294 (Integer format) 0 to 9.9999 x 10 ¹⁶ (Exponent format) 0 to 4294967294 (Integer format)	generating function:	Number G of stages fu	Generat unction		ndar	d
2.101 1.101 101 (2.).	0.0000 to 100.0000% (Percentage format)			$(^{7} + X^{6} + X^{6})$			
Error free interval (EFI):	0 to 4294967294 (Integer format) 0.0000 to 100.0000% (Percentage format)		10 X	$(^{9} + X^{5} + X^{10} + X^{7} + X^{7} + X^{9} + X^{$			
Frequency measurement (input clock) accuracy:	10,000,000 to 3,600,000,000 Hz ±10 ppm ± 1 kHz		15 X 23 X	$(^{15} + X^{14})$ $(^{23} + X^{18})$	+ 1 ITU-T recon + 1 ITU-T recon	nmen	ded O. 151 (1/2
Error performance:	ES; Errored Seconds			(³¹ + X ²⁸			
	EFS; Error Free Seconds SES; Severely Errored Seconds US; Unavailable Seconds	Mark ratio (variable): Mark ratio and number of bit shift:	1/2, 1/4, 1/ 1 bit	/8, 0/8,	, 1/2, 3/4, 7/8,	8/8	
	DM; Degraded Minutes	Programmable (PROG) p					
Threshold EI/EFI: B1 error (OPTION 71):	10° to 10° Available	Pattern length:	1 to 8,388,	608 (2 ²	23) bit		
		Pattern length and					
Measurement Timer		variable setting resolution [bit]:	Pattern	lenath	range	Sett	ing resolutior
Timer mode:	SINGLE, REPEAT, UNTIMED		1 to 262		.		1
Timer measurement period:	00 days 00 hours 00 minutes 01 seconds -		262,146				2
period.	99 days 23 hours 59 minutes 59 seconds		524,292 1,048,58				4 8
Measurement interval	-		2,097,16				16
timer:	0.1/1 s		4,194,33				32
Measurement time base:	±10 ppm (supplied by the D3371 main unit)	Zero substitution (ZSUB)	pattern		I		
Error Analysis (OPTION 7	2)	Pattern length: Continuous zero	2 [°] (n: 7, [•]	9, 10, ⁻	11, 15)		
Number of recording iterations:	1 to 131,071 point(s)	bit length and setting	70110 0-		Cantinua -		C
Result display format:	Time-series display (list format), statistics display (list format)	resolution [bit]:	ZSUB Pa length		Continuous ze bit length ran		Setting resolution
Automatic Search			2 ⁷ 2 ⁹		7 to 127 9 to 511		1 1
	Phase, threshold voltage, PRBS pattern		2 ¹⁰ 2 ¹¹		10 to 102 11 to 204		1 1
			2 ¹⁵		15 to 327		1
Synchronization		STM (SONET/SDH) patte					
Synchronization threshold Mode:	Automatic/manual	Frame structure: Number of frames:	STM-4, S				
Manual setting range:	PROG pattern; 10 ⁿ (n: 2, 3, 4, 5, 6, 7, 8, 9, 10)	Number of frames:			7 frames 6 frames		
Automatic synchronization:	PRBS pattern; 10" (n: 2, 3, 4, 5, 6, 7)	Payload types:	Can be s		d from PROG	patte	ern and PRBS
Re-synchronization	. 1 53. 03EI 3EIELIADIE	Scrambling:	pattern Can be p	provide	ed		
(manual):	Yes. User selectable	B1 byte:	Can be p				
Error Detection		Flexible (FLEX) pattern (127 tupos		
Mode		Number of patterns:	PROG pa		127 types 1 type		
Omitting/Inserting/Total:	inserting error (1's error), and total error	Pattern length:	PROG pa	PROG pattern; 128 to 65,536 bits (setting resolution; 64 bits)			
Overhead/Payload/Total:	Overhead error, payload error and total error (OPTION 71)				128 to 2,097,1 tion; 64 bits)	52 b	its
Specific/Other/Total:	Specific field error, not specific field error and total error	Number of combined patterns:	1 to 102	4 patte	ern(s)		
Measurement Mask		Pattern logic:	Can be l	logicall	y inverted		
Mask route:	1 to 16 (can be set to any value in increment of 1/16 bit route)	Burst					
		Mode:	External	l (the b	ourst input is a	vaila	able)
		Trigger					
		Mode:	Pattern	phase	d form 1/16 cl (fixed), Frame OPTION 71)		
		Flexible (OPTION 71):			or High level	can b	be set for each

Clock Input

Frequency:	10 MHz to 3.6 GHz
Termination and coupling:	DC termination, AC coupling
Input amplitude:	0.3 to 2 Vp-p
Input waveform:	Rectangular wave or Sine wave
	(175 MHz to 3.6 GHz)
	Rectangular wave (10 to 175 MHz)
Duty ratio:	50 ± 5%
Clock delay:	±1 ns (setting resolution; 1 ps)
Input impedance:	50Ω (nominal)
Termination voltage:	To GND: 0 V
Ũ	ECL (to -2 V);
	-2.3 to -1.7 V setting resolution: 50 mV
	PECL (to +3 V);
	+2.7 to +3.3 V setting resolution: 50 mV
	LVPECL (to +1.3 V);
	+1 to +1.6 V setting resolution: 50 mV
	CML (to Vcc);
	0 to 3.5 V setting resolution: 50 mV
Polarity:	Can be inverted
Connector:	SMA female

Data Input

Frequency:	10 MHz to 3.6 GHz
Mode:	NRZ
Termination and coupling:	DC termination, DC coupling
Input amplitude:	0.3 to 2 Vp-p
Threshold voltage:	To GND;
	-2.040 to +2.040 V setting resolution: 1 mV ECL (to -2 V);
	-1.850 to -0.750 V setting resolution: 1 mV PECL (to +3 V);
	3.150 to +4.250 V setting resolution: 1 mV LVPECL (to +1.3 V);
	+1.450 to +2.550 V setting resolution: 1 mV CML (to Vcc);
	Vcc -1.1 to Vcc +0.1 V setting resolution:
	1 mV (Vcc: termination voltage)
Termination voltage:	To GND: 0 V
5	ECL (to -2 V);
	-2.3 to -1.7 V setting resolution: 50 mV
	PECL (to +3 V);
	+2.7 to +3.3 V setting resolution: 50 mV
	LVPECL (to +1.3 V);
	+1 to +1.6 V setting resolution: 50 mV
	CML (to Vcc);
	0 to 3.5 V setting resolution: 50 mV
Input impedance:	50Ω (nominal)
Polarity:	Can be inverted
Connector:	SMA female

Burst (Trigger) Input

 Input level:
 0/-1 V

 Input impedance:
 50Ω (nominal) to 0V

 Connector:
 SMA female

Error Output

Output level:	
Load impedance:	
Connector:	

Trigger Output

Output level: Load impedance: Connector:

General Descriptions

+5 to +40°C
Relative humidity;
40 to 85% (without condensation)
-20 to +70°C
Relative humidity;
30 to 85% (without condensation)
90 VA or below
6 kg (13.2 lbs.) or less

0/-1 V50 Ω to 0 V SMA female

0/-1 V 50Ω to 0 V

SMA female

3.6 GHz Synthesizer Module (OPTION 13)

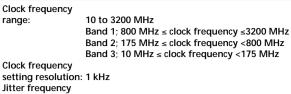
Clock Signal Source

10 MHz to 3.6 GHz
1 kHz
Within ±2 ppm
-85 dBc/Hz or less (10 kHz offset)
Yes. See below for specifications
1.2 ±0.6 Vp-p (175 MHz ≤f ≤3.6 GHz)
0.7 ±0.4 Vp-p (10 MHz ≤f ≤3.6 GHz)
Sine wave (175 MHz $\leq f \leq 3.6$ GHz)
Square wave (10 MHz ≤f <175 MHz)
50Ω
SMA female
en outputting the internal reference signal)
10 MHz
Within ±2 ppm
0 dBm ±5 dB
AC
SMA female
inputting the external reference signal)
10 MHz
$0 \text{ dBm} \pm 5 \text{ dB}$
AC
SMA female
Sima remaie
S
+5 to +40°C
Relative humidity;
40 to 85% (without condensation)
-20 to +70°C
Relative humidity;
30 to 85% (without condensation)
80 VA or below
3.5 kg (7.7 lbs.) or less

Jitter Tolerance (OPTION70)

Available option configurations table

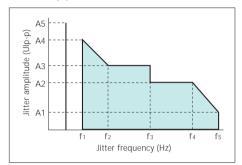
Jitter Generation



range: 10 Hz to 20 MHz (Band 1) 10 Hz to 5 MHz (Band 2) 10 Hz to 2 MHz (Band 3) Jitter frequency setting resolution: 10 Hz Jitter amplitude

range:

0 to 800 Ulp-p (Band 1, Band 2) 0 to 200 Ulp-p (Band 3)



Jitter	f ₀	f ₁	f ₂ to f ₃	f_3 to f_4	f₅			
frequency [Hz]	10	20	200 to 5 k	5 to 300 k	20 N			
Maximum Jitter	A5	A4	A3	A2	A1			
amplitude [Ulp-p]	800	500	50	20	0.3			
Band 2 (175 MHz ≤ clock frequency ≤800 MHz)								
Jitter	f ₀	f ₁	f ₂ to f ₃	f ₃ to f ₄	f₅			
frequency [Hz]	10	20	200 to 5 k	5 to 125 k	5 M			
Maximum Jitter amplitude [Ulp-p]	A5	A4	A3	A2	A1			
	800	500	50	20	0.5			
Band 3 (10 MHz \leq clock frequency \leq 175 MHz)								
Jitter	f _o	f ₁	f ₂ to f ₃	f ₃ to f ₄	f₅			
frequency [Hz]	10	20	200 to 5 k	5 to 200 k	2 M			
Maximum Jitter amplitude [Ulp-p]	A 5	A4	A3	A2	A1			
	000	120	12	5	0.5			

Jitter amplitude accuracy:

Jitter amplitude setting resolution:

A reference	standard;	ITU-T	0.172

1:	Jitter amplitude setting range	Setting resolution
Band 1 Band 2	0 to 5 Ulp-p 5 to 50 Ulp-p 50 to 500 Ulp-p 500 to 800 Ulp-p	0.01 Ulp-p 0.1 Ulp-p 1 Ulp-p 2 Ulp-p
Band 3	0 to 1 Ulp-p 1 to 10 Ulp-p 10 to 100 Ulp-p 100 to 200 Ulp-p	0.01 Ulp-p 0.1 Ulp-p 1 Ulp-p 2 Ulp-p

Jitter Tolerance Measurement

Measurement mode:

Can be selected from the following modes Search mode; Jitter tolerance points are searched automatically Sweep mode; Jitter tolerance at specified points are measured

	/	, 10/17	~~~	3	10	.n/
Configurations	OPT	ION TOINT	ION 12 OPT	ION 13 OPT	ION TO OPT	ION TI OPT
No. 1	NO	YES	NO	NO	NO	NO
No. 2	NO	YES	NO	NO	NO	YES
No. 3	YES	NO	YES	NO	NO	NO
No. 4	YES	NO	YES	NO	YES	NO
No. 5	YES	YES	YES	NO	NO	NO
No. 6	YES	YES	YES	YES	NO	NO
No. 7	YES	YES	YES	NO	YES	NO
No. 8	YES	YES	YES	NO	NO	YES
No. 9	YES	YES	YES	YES	YES	NO
No. 10	YES	YES	YES	YES	NO	YES
No. 11	YES	YES	YES	NO	YES	YES
No. 12	YES	YES	YES	YES	YES	YES

Please contact our office for other configurations.

Module options

OPTION 13:	3.6 GHz synthesizer module
OPTION 12:	Error Detector module
OPTION 11:	Pulse Pattern Generator (3 Vp-p output) module
OPTION 10:	Pulse Pattern Generator (2 Vp-p output) module

Measurement function options

OPTION 70:	Jitter Tolerance option
OPTION 71:	Pattern option
OPTION 72:	Error phase analysis option







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Please be sure to read the product manual thoroughly before using the products. Specifications may change without notification.

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